IT IS CLAIMED:

1. A non-volatile memory comprising:

a plurality of storage units formed upon a substrate and arranged into a plurality of columns connected along respective bit lines each comprising a number of said storage units connected in series between a first select transistor and a second select transistor, whereby said storage units form a corresponding number of rows and wherein the columns are subdivided into a plurality of distinct subsets;

a number of word lines each connecting the storage elements of a corresponding row; and

biasing circuitry connected to the select transistors, wherein the voltage level on the gates of the first select transistors in one subset can be set independently of the voltage level on the gates of the first select transistors in the other subsets and the voltage level on the gates of the second select transistors in one subset can be set independently of the voltage level on the gates of the second select transistors in the other subsets.

2. The non-volatile memory of claim 1, wherein each of said subsets of columns are formed upon a distinct contiguous region of the substrate.

3. The non-volatile memory of claim 2, wherein the regions are each formed upon a corresponding well structure connected to said biasing circuitry wherein the voltage level in the well structure in one region can be set independently of the voltage level in the well structure in the other regions.

4. The non-volatile memory of claim 1, wherein the source side of the bit lines of each subset are connected to a corresponding common source line connected to said biasing circuitry wherein the voltage level on the common source line in one subset can be set independently of the voltage level on the common source line in the other subsets.

5. The non-volatile memory of claim 4, wherein said storage units comprise floating gate memory cells and the word lines are connected to the control gates of the memory cells of the respective row.

6. The non-volatile memory of claim 4, wherein said storage units are multi-state storage units.

7. The non-volatile memory of claim 4, further comprising:

erase circuitry coupled to said plurality of storage units, wherein the number of storage units in said plurality of storage units corresponds to the size of the erase unit of the non-volatile memory.

8. The non-volatile memory of claim 7, wherein the number of columns in each of said subsets is based on the size of the data transfer unit between the non-volatile memory and a host to which it is connectable.

9. The non-volatile memory of claim 1, further comprising:

a read circuit connected to the word lines to set voltages levels thereon in a read process; and

a plurality of sets of one or more read registers connectable to the columns for storing the data content from a storage element in a column to which the register is connected during a read process.

10. The non-volatile memory of claim 9, wherein each column has a respective set of one or more read registers.

11. The non-volatile memory of claim 9, wherein each set of one or more read registers is connectable to a plurality of columns.

12. The non-volatile memory of claim 9, further comprising:

program circuitry connected to the word lines to set voltages levels thereon in a write process; and

a plurality of sets of one or more write registers connectable to the columns for storing the data content to be written in a storage element in a column to which the register is connected during a read process.

13. The non-volatile memory of claim 12, wherein the read registers are the same as the write registers.

14. A method of operating a non-volatile memory, the memory comprising a plurality of storage units formed upon a substrate and arranged into a plurality of columns connected along respective bit lines each comprising a number of said storage units connected in series between a first select transistor and a second select transistor, whereby said storage units form a corresponding number of rows with a respective wordline connecting the storage elements of each row and wherein the columns are subdivided into a plurality of distinct subsets, the method comprising:

setting a voltage level on the drain side of a first bit line in a first of the subsets;

setting voltage levels on the word lines;

setting voltage levels concurrently on the gates of the first and second select transistors in said first and a second of the subsets, wherein the voltage levels on the gates of the select transistors in second subset is different than the voltage levels on the gates of the select transistors the first subset.

15. The method of claim 14, wherein said setting voltage levels on the drain side of the first bit line and said setting voltage levels on the gates of the select transistors are performed prior to said setting voltage levels on the word lines.

16. The method of claim 15, wherein the method is part of a read process.

17. The method of claim 16, wherein the voltage level on the drain side first bit line is a value in the range of from 0.5 to 0.7 volts, the voltage level on a first of said word lines is data dependent, and the voltage level on the other word lines is a value in the range of from 4 to 5 volts.

18. The method of claim 17, wherein the source side of the columns of first subset are set to ground and the source side of the columns of second subset are set to the high logic level.

19. The method of claim 18, wherein the voltage level on the gate of the drain side select transistors of the first set is set to a value in the range of from 4 to 5 volts, the voltage level on the gate of the drain side select transistors of the second set is set to ground, the voltage level on the gate of the source side select transistors of the first set is set to the high logic level, and the voltage level on the gate of the source side select transistors of the second set is initially set to a value higher than to the high logic level and lowered to the high logic level concurrently with said setting voltage levels on the word lines.

20. The method of claim 19, wherein the voltage level on the drain side of the bit lines in the second subset is set to ground.

21. The method of claim 16, wherein the read process is part of a verify process.

22. The method of claim 15, wherein the method is part of a write process.

23. The method of claim 22, wherein the voltage level on the drain side of the first bit line is set to ground, the voltage level set on a first of said word lines a programming voltage.

24. The method of claim 23, wherein the voltage level on the word lines in the rows non-adjacent to the first wordline is set to a value in the range of from 8 to 12 volts.

25. The method of claim 24, wherein the voltage level on the word lines in the rows adjacent to the first wordline are set to a value in the range of from 8 to 12 volts.

26. The method of claim 24, wherein the voltage level on the word line in a first row adjacent to the first wordline is set to a value in the range of from 8 to 12 volts and the voltage level on the word line in the second row adjacent to the first wordline is set to ground.

27. The method of claim 24, wherein the voltage level on the word lines in the rows adjacent to the first wordline are set to ground.

28. The method of claim 23, wherein the source side of the columns of the first and second subsets are set to the high logic level.

29. The method of claim 28, wherein the voltage level on the gate of the drain side select transistors of the first is set to the high logic level, the voltage level on the gate of the drain side select transistors of the second set is set to a value less than or equal to the high logic level, the voltage level on the gate of the source side select transistors of the first set is set to ground, and the voltage level on the gate of the source side select transistors of the second set is initially set to a value higher than to the high logic level and lowered to the high logic level concurrently with said setting voltage levels on the word lines.

30. The method of claim 29, wherein the voltage level on the drain side of the bit lines in the second subset is set the same value as the gate of the drain side select transistors of the second set.

31. The method of claim 23, wherein the voltage level on the drain side of a second bit line in the first of the subsets is set to the high logic level.

32. The method of claim 22, further comprising:

concurrently erasing the first and second subsets prior to said setting the voltages on the drain side of bit line in the first subset and on the gates of the first and second select transistors in said first and second subsets.

33. A non-volatile memory comprising:

a plurality of storage units formed upon a substrate and arranged into a plurality of columns connected along respective bit lines and forming one or more rows;

a plurality of well structures in the substrate upon which the storage units are formed wherein the storage units are subdivided into a plurality of subsets each formed upon a corresponding one of the well structures;

a plurality of word lines each connecting the storage elements of a respective row; and

a well control circuit connected to the substrate whereby the voltage level of the well structures can be independently controlled.

34. The non-volatile memory of claim 33, wherein the storage units are erasable through the well structures in the substrate.

35. The non-volatile memory of claim 34, wherein the subsets are erased together.

36. The non-volatile memory of claim 33, further comprising:

a read circuit connected to the word lines to set voltages levels thereon in a read process; and

a plurality of sets of one or more read registers connectable to the columns for storing the data content from a storage element in a column to which the register is connected during a read process.

37. The non-volatile memory of claim 36, wherein each column has a respective set of one or more read registers.

38. The non-volatile memory of claim 36, wherein each set of one or more read registers is connectable to a plurality of columns.

39. The non-volatile memory of claim 36, further comprising:

program circuitry connected to the word lines to set voltages levels thereon in a write process; and

a plurality of sets of one or more write registers connectable to the columns for storing the data content to be written in a storage element in a column to which the register is connected during a read process.

40. The non-volatile memory of claim 39, wherein the read registers are the same as the write registers.

41. The non-volatile memory of claim 33, wherein the storage units are floating gate memory cells and the word lines are connected to the control gates of the memory cells of the respective row.

42. The non-volatile memory of claim 41, wherein the storage units are arranged in a NAND structure.

43. The non-volatile memory of claim 41, wherein the storage units are arranged in a NOR structure.

44. The non-volatile memory of claim 33, wherein each of the storage units can store more than two data states.

45. A method of operating a non-volatile memory, the memory comprising a plurality of storage units formed upon a substrate and arranged into a plurality of columns connected along bit lines and forming one or more rows with a respective wordline connecting the storage elements of each row wherein the storage units are subdivided into a plurality of subsets each formed upon a corresponding well structure, the method comprising:

setting a voltage level on a bit line in a first of the subsets;

setting a voltage level on a first of the word lines;

setting a voltage level in the well structure of the first subset concurrently with said setting a voltage level on a first of the word lines; and

setting a voltage level in the well structure of a second subset concurrently with said setting a voltage level on a first of the word lines, wherein the voltage level in the well structure of the second subset is different than the voltage level in the well structure of the first subset.

46. The method of claim 45, wherein the method is part of a read process.

47. The method of claim 46, wherein the voltage on the bit line is precharged to a value in the range of from 0.5 to 0.7 volts, the voltage level on the first wordline is data dependent.

48. The method of claim 47, wherein the voltage level in the well structure of the first subset is set to ground.

49. The method of claim 48, further comprising:

setting a voltage level on the word lines other than said first word line, wherein the voltage level on the other word lines is a value in the range of from 4 to 5 volts.

50. The method of claim 46, wherein the read process is part of a verify process.

51. The method of claim 45, wherein the method is part of a write process.

52. The method of claim 51, wherein the voltage level on the first wordline is a programming voltage, the voltage on the bit line is set to ground.

53. The method of claim 52, wherein the voltage level in the well structure of the first subset is set to ground.

54. The method of claim 53, wherein the voltage level on the wordline in a first row adjacent to the first wordline is set to ground.

55. The method of claim 54, wherein the voltage level on the wordline in the second row adjacent to the first wordline is set to ground.

56. The method of claim 54, wherein the voltage level on the word line in the second row adjacent to the first wordline is a value in the range of from 8 to 12 volts.

57. The method of claim 54, wherein the voltage level on the word lines in the rows non-adjacent to the first wordline is a value in the range of from 8 to 12 volts.

58. The method of claim 51, further comprising:

concurrently erasing the first and second subsets prior to said setting the voltages on the bit line in the first subset, on the first wordline, and in the well structure of the first and second subsets.